## **Parallel Processing**

## Multiple Choice question & Answers:-

1) A collection of lines that connects several devices is called
A. bus
B. peripheral connection wires
C. Both a and b
D. internal wires
Answer: A. bus
2) A complete microcomputer system consist of
A. microprocessor
B. memory
C. peripheral equipment
D. all of the above
Answer: D. all of the above
3) PC Program Counter is also called
A. instruction pointer
B. memory pointer
C. data counter
D. file pointer

#### Answer: A. instruction pointer

4) In a single byte how many bits will be there?
A. 8
B. 16
C. 4
D. 32
Answer: A. 8
5) CPU does not perform the operation
A. data transfer
B. logic operation
C. arithmetic operation
D. all of the above
Answer: A. data transfer
6) The access time of memory is the time required for performing any single CPU operation.
A. Longer than
B. Shorter than
C. Negligible than
D. Same as

### Answer: A. Longer than

7) Memory address refers to the successive memory words and the machine is called as	
A. word addressable	
B. byte addressable	
C. bit addressable	
D. Terra byte addressable	•
Answer: A. word addressable	
3) A microprogram written as string of 0's and 1's is a	
A. Symbolic microinstruction	
B. binary microinstruction	
C. symbolic microinstruction	
D. binary micro-program	
Answer: D. binary micro-program	
A an automobile acombly line	
A. an automobile assembly line B. house pipeline	
C. both a and b	
D. a gas line	

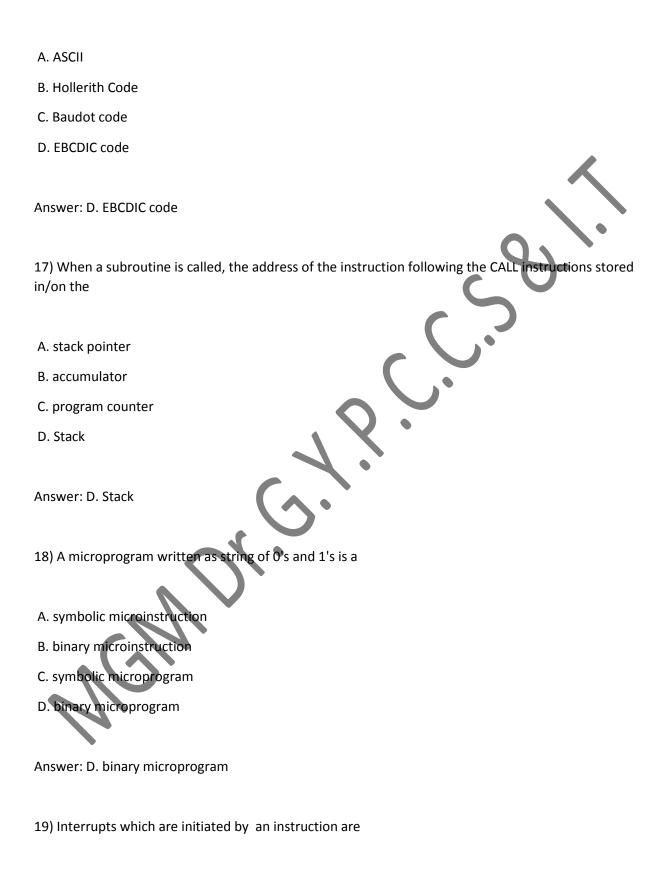
Answer: A. an automobile assembly line

10) Data hazards occur when
A. Greater performance loss
B. Pipeline changes the order of read/write access to operands
C. Some functional unit is not fully pipelined
D. Machine size is limited
Answer: B. Pipeline changes the order of read/write access to operands
11) Processors of all computers, whether micro, mini or mainframe must have
A. ALU
B. Primary Storage
C. Control unit
D. All of above
Answer: D. All of above
12) What is the control unit's function in the CPU?
A. To transfer data to primary storage
B. to store program instruction
C. to perform logic operations
D. to decode program instruction
Answer: D. to decode program instruction
13) What is meant by a dedicated computer?

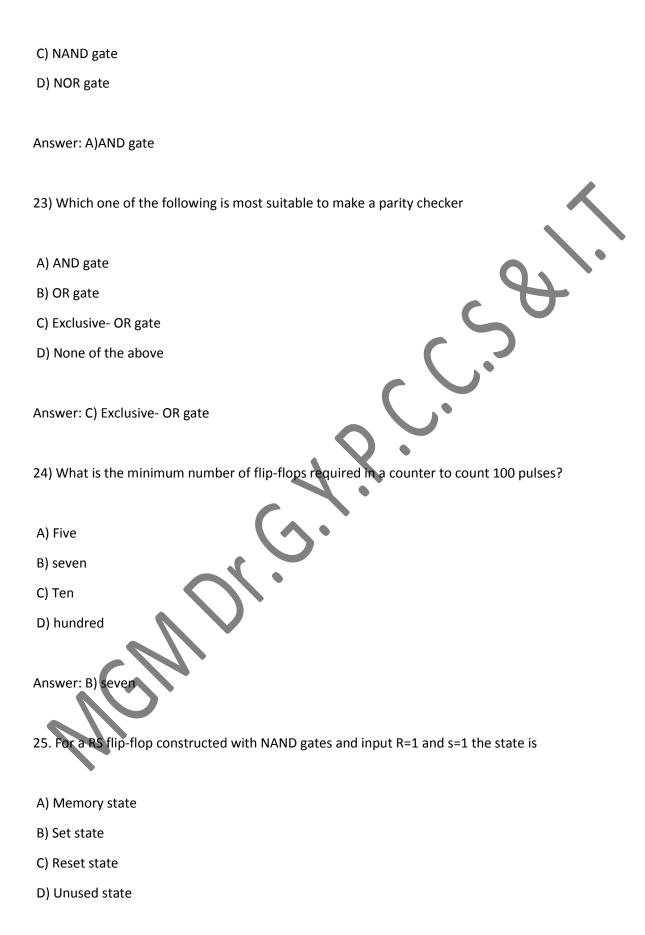
A. which is used by one person only
B. which is assigned to one and only one task
C. which does one kind of software
D. which is meant for application software only
Answer: B. which is assigned to one and only one task
14) The most common addressing techiniques employed by a CPU is
44
A. immediate
B. direct
C. indirect
D. register
E. all of the above
Answer: E. all of the above
15) Pipeline implement
A. fetch instruction
B. decode instruction
C. fetch operand
D. calculate operand
E. execute instruction
F. all of abve

16) Which of the following code is used in present day computing was developed by IBM corporation?

Answer: F. all of abve



A. internal
B. external
C. hardware
D. Software
Answer: B. external
20) Memory access in RISC architecture is limited to instructions
A. CALL and RET
B. PUSH and POP
C. STA and LDA
D. MOV and JMP
Answer: C. STA and LDA
21) From where interrupts are generated?
A) Central processing unit
B) Memory chips
C) Registers
D) I/O devices
Answer: D) I/O devices
22) The output of a gate is low when at least one of its input is low . It is true for
A) AND gate
B) OR gate



Answer: D) Unused state

26. The advantage of RISC processor over CISC processor is that

- A) The hardware architecture is simpler
- B) An instruction can be executed in one cycle
- C) Less number of registers accommodate in chip
- D) Parallel execution capabilities

Answer: B) An instruction can be executed in one cycle

27. Which of the following is true about interrupts?

- A) They are generated when memory cycles are stolen
- B) They are used in place of data channels
- C) They can be generated by arithmetic operation
- D) They can indicate completion of an I/O operation

Answer: A) They are generated when memory cycles are stolen

28. Te devices connected to a microprocessor can use the data bus:

- A) all the time
- B) at regular interval of time
- C) only when it's sending or receiving data
- D) when the microprocessor is reset

Answer: C) only when it's sending or receiving data

29. Intel 8080 microprocessor has an instruction set of 91 instruction. The opcode to implement this instruction set should be at least

- A) 3 bit long
- B) 5 bit long
- C) 7 bit long
- D) 9 bit long

Answer: C) 7 bit long

30. Dynamic RAMs are best suited to

- A) slow system
- B) large system
- C) one bit system
- D) none of the above

Answer: A) slow system

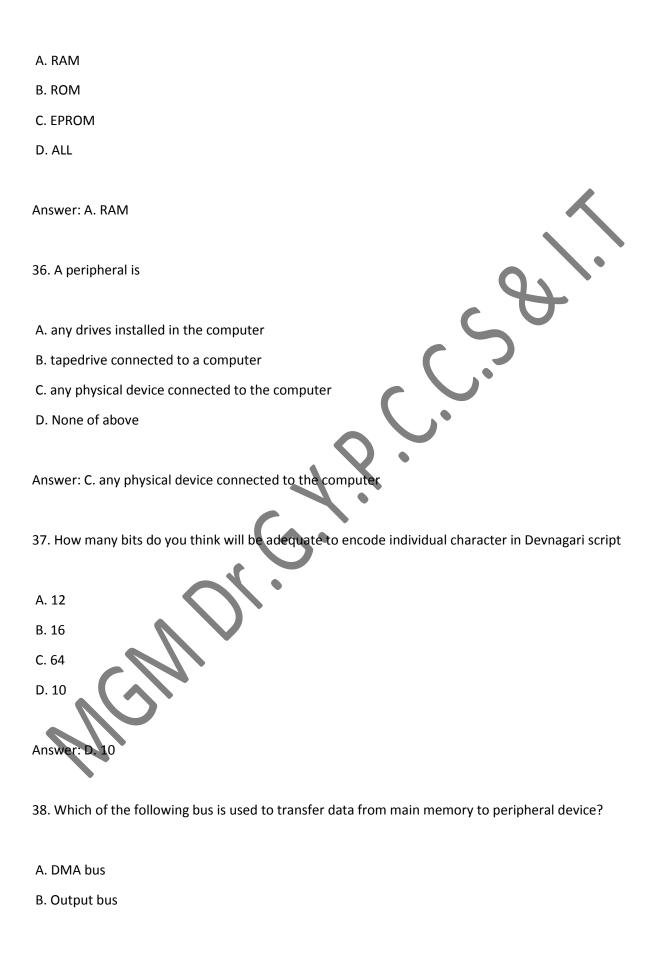
31. Intel Pentium CPU is a

- A. RISC based
- B. CISC based
- C. Both of the above
- D. None of the above

Answer: A. RISC based

# 32. A modem is used to link up two computers via A. telephone line B. dedicated line C. Both of the above D. None of the above Answer: C. Both of the above 33. The maximum integer which can be stored on a 8 bit accumulator is A. 112 B. 200 C. 255 D. 224 Answer: C. 255 34. In a system with a 16 bit address bus, what is the maximum number of 1K byte memory devices it could contain A. 16 B. 64 C. 256 Answer: C. 256

35. Which of the following memories in a computer is volatile?



C. Data bus D.All of the above Answer: C. Data bus 39. To provide increased memory capacity for operating system, the A. virtual memory is created B. cache memory is increased C. memory for OS is reserved D. Additional memory is installed Answer: A. virtual memory is created 40. CD -RAW is A. Input device only B. output device only C. Both of the above D. None of the above Answer: B. output device only 41. Which of the following require large computer memory?

A. Imaging

B. Graphics

D. All of the above

C. Voice

#### Answer: D. All of the above

- 42. Which major development led to the production of microcomputers?
- A. Magnetic disks
- B. floppy disks
- C. Logic gates
- D. Integrated Circuits

Answer: D. Integrated Circuits

- 43. In immediate addressing the operand is placed
- A. in the CPU register
- B. after opcode in the instruction
- C. in the memory
- D. in the stack

Answer: B. after opcode in the instruction

- 44. Micro instructions are stored in
- A. computer memory
- B. primary storage
- C. secondary storage
- D. control memory
- E. cache memory

#### Answer: D. control memory

#### 45. Pipeline processing implement

- A. fetch instruction
- B. decode instruction
- C. fetch operand
- D. calculate operand
- E. execute instruction
- F. all of the above

Answer: F. all of the above

46. The 16- bit registers in 8085 is

- A. general purpose register
- B. accumulator
- C. stack pointer and program counter
- D. all of the above

Answer: C. stack pointer and program counter

47. Instruction pipelining has minimum stages

- A. 4
- B. 2
- C. 3
- D. 6

48. S\	/stems	that c	lo not h	ave pa	arallel i	processing	capabilit	ies are

- A. SISD
- B. SIMD
- C. MIMD
- D. All of the above

Answer: A. SISD

49. The word size of the microprocessor refers to

- A. the amount of a information that can be stored in a byte
- B. the amount of a information that can be stored in a cycle
- C. The number of machine operations performed in a second
- D. the maximum length of an English word that can be input to a computer

Answer: B. the amount of a information that can be stored in a cycle

50. How many address lines are needed to address each memory location in a 2048X 4 memory chip?

A. 10

B. 11

C. 8

D. 12

Answer: B. 11

51. Who is regarded as the founder of Computer Architecture?
A. Alan Turing
B. Konrad Zuse
C. John von Neumann
D. John William Mauchly
E. None of the answers above is correct
Answer: C. John von Neumann
52. What is characteristic for the organization of a computer architecture?
A. Size
B. Dynamic behaviour
C. Static behaviour
D. Speed
E. None of the answers above is correct
Answer: B. Dynamic behaviour
53. What is usually regarded as the von Neumann Bottleneck?
A. Processor/memory interface  B. Control unit
C. Arithmetic logical unit
D. Instruction set
E. None of the answers above is correct
Answer: A. Processor/memory interface

54. How does the number of transistors per chip increase according to Moore 's law?
A. Quadratically
B. Linearly
C. Cubicly
D. Exponentially
E. None of the answers above is correct
Answer: D. Exponentially
55. Who is regarded as the founder of Computer Science?
A. Alan Turing
B. Konrad Zuse
C. J. Presper Eckert
D. John William Mauchly
E. None of the answers above is correct
Answer: A. Alan Turing
56. Which is the fastest storage unit in a usual memory hierarchy?  A. Cache
B. Main memory
C. Hard disk
D. Register
E. None of the answers above is correct

57. Which cache miss does not occur in case of a fully associative cache?

- A. Conflict miss
- B. Capacity miss
- C. Compulsory miss
- D. Cold start miss
- E. None of the answers above is correct

Answer: A. Conflict miss

58. Which miss even occurs in infinite caches?

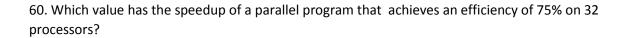
- A. Coherence miss
- B. Capacity miss
- C. Conflict miss
- D. Cold start miss
- E. None of the answers above is correct

Answer: D. Cold start miss

59. What is stored in a Translation Lookaside Buffer?

- A. System dumps
- B. Physical addresses
- C. rogram data
- D. Operating system log files
- E. None of the answers above is correct

#### Answer: B. Physical addresses



- A. 18
- B. 24
- C. 16
- D. 20
- E. None of the answers above is correct

Answer: B. 24

61. Pipelining strategy is called implement

- A. instruction execution
- B. instruction prefetch
- C. instruction decoding
- D. instruction manipulation

Answer: B. instruction prefetch

62. The concept of pipelining is most effective in improving performance if the tasks being performed in different stages :

- A. require different amount of time
- B. require about the same amount of time
- C. require different amount of time with time difference between any two tasks being same

D. require different amount with time difference between any two tasks being different

Answer: B. require about the same amount of time

63) Which Algorithm is better choice for pipelining?

- A. Small Algorithm
- B. Hash Algorithm
- C. Merge-Sort Algorithm
- D. Quick-Sort Algorithm

Answer: C. Merge-Sort Algorithm

64. The expression 'delayed load' is used in context of

- A. processor-printer communication
- B. memory-monitor communication
- C. pipelining
- D. none of the above

Answer: C. pipelining

65. Parallel processing may occur

- A. in the instruction stream
- B. in the data stream
- C. both[A] and [B]
- D. none of the above

#### Answer: C. both[A] and [B]

66. The cost of a parallel processing is primarily determined by :

- A. Time Complexity
- B. Switching Complexity
- C. Circuit Complexity
- D. None of the above

Answer: C. Circuit Complexity

67. An instruction to provide small delay in program

- A. LDA
- B. NOP
- C. BEA
- D. None of the above

Answer: B. NOP

68. Characteristic of RISC (Reduced Instruction Set Computer) instruction set is

- A. three instructions per cycle
- B. two instructions per cycle
- C. one instruction per cycle
- D. none of the

Answer: C. one instruction per cycle

69. In daisy-chaining priority method, all the devices that can request an interrupt are connected in
A. parallel
B. serial
C. random
D. none of the above
Answer: B. serial
70. Which one of the following is a characteristic of CISC (Complex Instruction Set Computer)
A. Fixed format instructions
B. Variable format instructions
C. Instructions are executed by hardware
D. None of the above
Answer: B. Variable format instructions
71. During the execution of the instructions, a copy of the instructions is placed in the
A. Register
B. RAM
C. System heap  D. Cache
Answer: D. Cache

execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?
A. A
B. B
C. Both take the same time
D. Insuffient information
Answer: A. A
73. A processor performing fetch or decoding of different instruction during the execution of another instruction is called
A. Super-scaling
B. Pipe-lining
C. Parallel Computation
D. None of these
Answer: B. Pipe-lining
74. For a given FINITE number of instructions to be executed, which architecture of the processor
provides for a faster execution ?
A. ISA
B. ANSA
C. Super-scalar
D. All of the above
Answer: C. Super-scalar

72. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can

75. The clock rate of the processor can be improved by,

A. Improving the IC technology of the logic circuits

B. Reducing the amount of processing done in one step

C. By using overclocking method

D. All of the above

Answer: D. All of the above

76. An optimizing Compiler does,

A. Better compilation of the given piece of code.

B. Takes advantage of the type of processor and reduces its process time.

C. Does better memory managament.

D. Both a and c

Answer: B. Takes advantage of the type of processor and reduces its process time.

77. The ultimate goal of a compiler is to,

A. Reduce the clock cycles for a programming task.

B. Reduce the size of the object code.

C. Be versatile.

D. Be able to detect even the smallest of errors.

Answer: A. Reduce the clock cycles for a programming task.

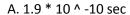
78. SPEC stands for,

A. Standard Performance Evaluation Code.
B. System Processing Enhancing Code.
C. System Performance Evaluation Corporation.
D. Standard Processing Enhancement Corporation.
Answer: C. System Performance Evaluation Corporation.
79. As of 2000, the reference system to find the performance of a system is
A. Ultra SPARC 10
B. SUN SPARC
C. SUN II
D. None of these
Answer: A. Ultra SPARC 10  80. When Performing a looping operation, the instruction gets stored in the
A. Registers B. Cache C. System Heap D. System stack  Answer: B. Cache
81. The average number of steps taken to execute the set of instructions can be made to be less than one by following

- A. ISA
- B. Pipe-lining
- C. Super-scaling
- D. Sequential

Answer: C. Super-scaling

82. If a processor clock is rated as 1250 million cycles per second, then its clock period is \_



Answer: D. 8 \* 10 ^ -10 sec

83. If the instruction, Add R1,R2,R3 is executed in a system which is pipe-lined, then the value of S is (Where S is term of the Basic performance equation)

- A. 3
- B. ~2
- C. ~1
- D. 6

Answer: C. ~1

84. CISC stands for,

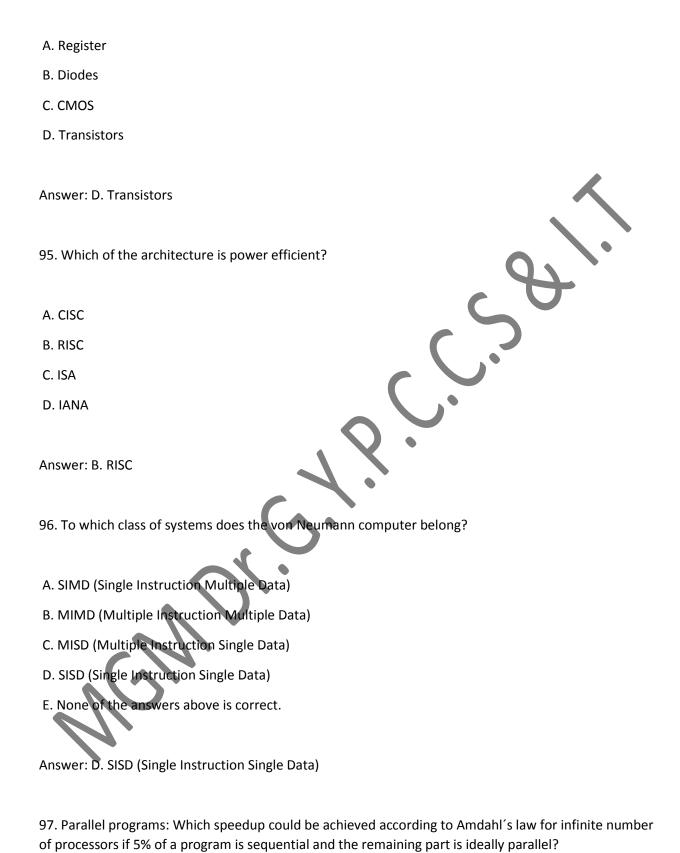
A. Complete Instruction Sequential Compilation

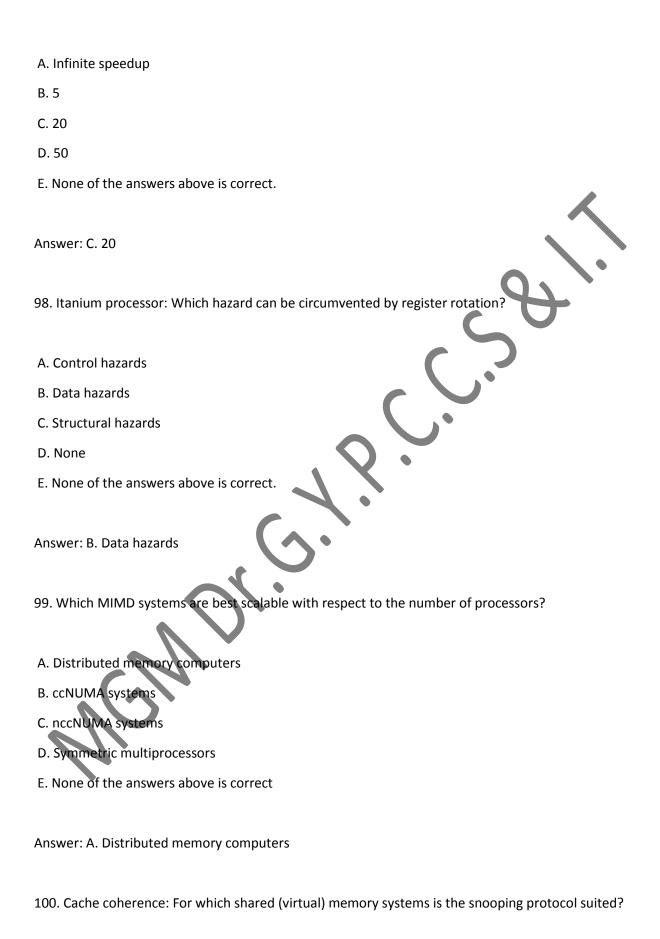
B. Computer Integrated Sequential Compiler
C. Complex Instruction Set Computer
D. Complex Instruction Sequential Compilation
Answer: C. Complex Instruction Set Computer
85. As of 2000, the reference system to find the SPEC rating are built with Processor.
A. Intel Atom SParc 300Mhz
B. Ultra SPARC -IIi 300MHZ
C. Amd Neutrino series
D. ASUS A series 450 Mhz
Answer: B. Ultra SPARC -IIi 300MHZ
86. The CISC stands for
A. Computer Instruction Set Compliment
B. Complete Instruction Set Compliment
C. Computer Indexed Set Components
D. Complex Instruction set computer
Answer: D. Complex Instruction set computer
87. The computer architecture aimed at reducing the time of execution of instructions is
A. CISC
B. RISC
C. ISA

D. ANNA
Answer: B. RISC
88. The Sun micro systems processors usually follow architecture.
A. CISC
B. ISA
C. ULTRA SPARC
D. RISC
Answer: D. RISC
89. The RISC processor has a more complicated design than CISC.
A. True
B. False
Answer: B. False
90. The iconic feature of the RISC machine among the following are
a) Reduced number of addressing modes
b) Increased memory size
c) Having a branch delay slot
d) All of the above

Answer: c) Having a branch delay slot

91. Both the CISC and RISC architectures have been developed to reduce the
A. Cost
B. Time delay
C. Semantic gap
D. All of the above
Answer: C. Semantic gap
92. Out of the following which is not a CISC machine.
A. IBM 370/168
B. VAX 11/780
C. Intel 80486
D. Motorola A567
Answer: D. Motorola A567
93. Pipe-lining is a unique feature of
A. RISC
B. CISC
C. ISA D. IANA
Answer: A. RISC
94. In CISC architecture most of the complex instructions are stored in





- A. Crossbar connected systems
- B. Systems with hypercube network
- C. Systems with butterfly network
- D. Bus based systems
- E. None of the answers above is correct.

Answer: D. Bus based systems